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# Low Power Dynamic CMOS Full-Adder Cell

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***Abstract* — In this paper a new area efficient, high-speed and ultra-low power 1-bit full adder cell is presented. The performance: power, time delay and power delay product (PDP) of the proposed adder cell has been analyzed in comparison with the four existent low-power, high-speed adders. The circuits being studied are optimized for energy efficiency at 0.18-µm CMOS process technology and intensive simulation runs on Cadence environment shows that the new full adder has more than 16% in power savings over C-CMOS full adder.**

*Keywords*— **Low-Power, Full-Adder, CMOS.**

## I. INTRODUCTION

Most of the VLSI applications, such as digital signal processing, image and video processing, and microprocessors, extensively use arithmetic operations. Additions, subtraction, multiplication, division, address calculation, and multiply and accumulate (MAC) are examples of the most commonly used operations [1-3]. Addition is one of the fundamental arithmetic operations and the 1-bit full-adder cell is the building block of all those modules in additions to its main task, which is adding two binary numbers. In most of these systems the adder is part of the critical path that determines the overall performance of the system and full adder is the core element of complex arithmetic circuits. That is why enhancing its performance is critical to improve the overall module performance. One of the objectives of our work is to design a circuit based on 0.18-µm CMOS process technology that can operate in ultra-low power supply voltage. This full adder has a simple structure but it operates very well and causes remarkable advances in reducing power in comparison with other well-known designs. This reduction is due to simple structure and reduced number of transistors.

The rest of this paper is organized as follows: in Section II we review some existent implementations of the full-adder cell. Then in Section III, we present the novel 1-bit dynamic full-adder cell and analyze its performance. In Section IV, we present simulation results, which show the superiority of the proposed cell. Finally, Section V concludes the paper.

## II. REVIEW OF FULL ADDER DESIGNS

Several variants of CMOS logic styles have been used to implement low-power full adder cells [4-7]. They are built upon different logic styles. Among these adders, the circuits shown in Fig.1 will be used for comparison in this paper. Although all of them do the similar function, but the ways that they produce the intermediate nodes and the outputs, the loads on the inputs, and the transistor count are varied. Different logic styles tend to favor one performance aspect at the expense of the other. Some of them use one logic style for the whole full adder and the others use more than one logic style for their implementation. These full adders have been introduced in different works up to now. The studies and simulation results show that each of them has some strength and some weaknesses points. In the following, a brief description of each full adder is prepared.

The complementary CMOS full adder (C-CMOS) [8] as shown in Fig. 1(a) is based on regular CMOS structure with conventional pull-up and pull-down transistors and has 28 transistors. C-CMOS generates $C_{out}$ throughout a single static CMOS gate. The input capacitance of a static CMOS gate is large because each input is connected to the gate of at least a PMOS and a NMOS device. Additional buffers at the last stage are needful to provide the required driving power because the series transistors in the output stage form a weak driver. Another problem that is sole in CMOS is that there is an extra delay caused by generating the *sum* using the $C_{out}$ signal as an input. The other adder cells try to balance the generation of both signals. The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing.

Another conventional adder, shown in Fig. 1(b) is the Complementary Pass Transistor Logic (CPL) [8] with swing restoration. It uses 32 transistors. CPL produces many intermediate nodes and their complement to make the outputs. The basic difference between the pass-transistor logic and the complementary CMOS logic styles is that the source side of the pass logic transistor network is connected to some input signals instead of the power lines. One pass-transistor network is enough to implement the logic function therefore; results are generated by smaller number of transistors and smaller input load. When the transistor gates are oversized a problem, which is overloading the inputs occurs and creates high capacitance values. This problem occurs in CPL and CMOS. Pass-transistor logic has an intrinsic problem which is threshold voltage drop. So, output inverters are necessary to guarantee the drivability. CPL is not an appropriate choice for low power due its high switching activity of intermediate nodes, its high transistor count, its static inverters and overloading of its inputs. But, CPL is better than CMOS for the studied circuit conditions. So both circuits will be considered for comparison in this paper.

Hybrid full adder [9] has been shown in Fig. 1(c). In this design the pass logic circuit that cogenerates the

intermediate *XOR* and *XNOR* outputs has been improved. This full adder cell can work at low supply voltage. It uses 26 transistors but has the full swing logic, balanced output and good output drivability.

The 10-Transistors full adder (10T) Fig. 1(d) uses hybrid logic style [10]. It has small transistor count but it is not full swing. This full adder suffers from the lack of driving capabilities in fan-out situation and the performance of it degrades dramatically when they are cascaded. This full adder generates A⊕B and uses it and its complement as a select signal to generate the outputs. It enjoys small transistor count and exploits the non-full swing pass transistors with swing restored transmission gate techniques. It must be notified that this full adder cannot work properly when supply voltage is less than 1.8V.

The 4-Transistors full adder cell (4T) Fig.1(e) eliminates time consuming XOR gates and it is based on Majority Function [11]. This design enjoys low power and high performance due to its transistor count and it can work at supply voltage as low as 0.65V but it also suffers from the point of area due to the use of capacitors in its design. Many full adder designs based on Majority Function have been proposed [12-14], but they are not comparable from the point of power consumption with 4T, because 4T has the smallest transistor count and it employs only two simple classical CMOS inverter in its design.

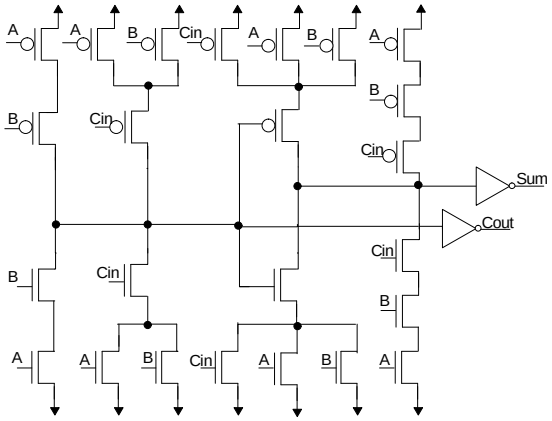


Fig. 1(a). The conventional CMOS full adder (CCMOS)

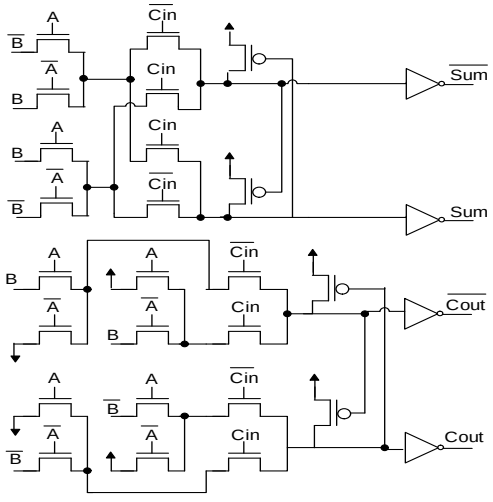


Fig. 1(b). The complementary pass transistor logic adder (CPL)

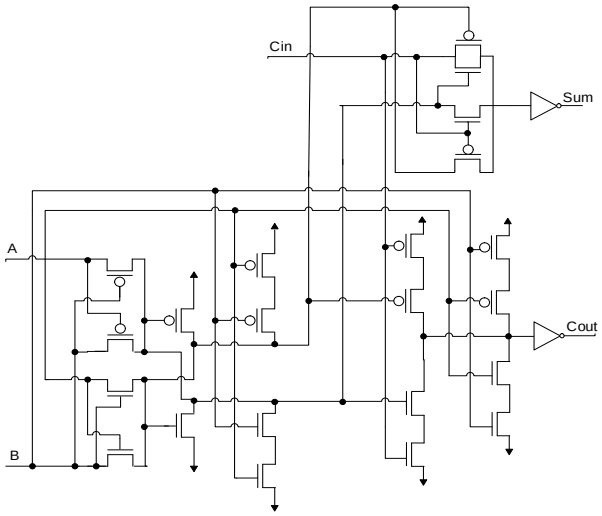


Fig. 1(c). The Hybrid Full Adder

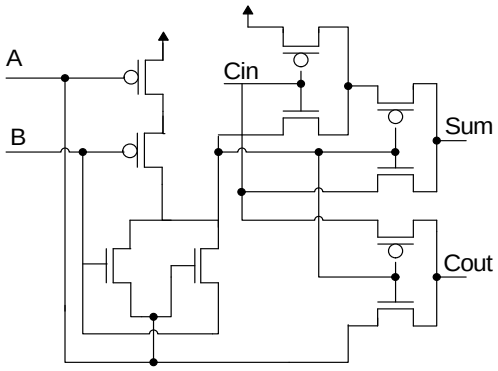


Fig. 1(d). The 10-Transistor full adder (10T)

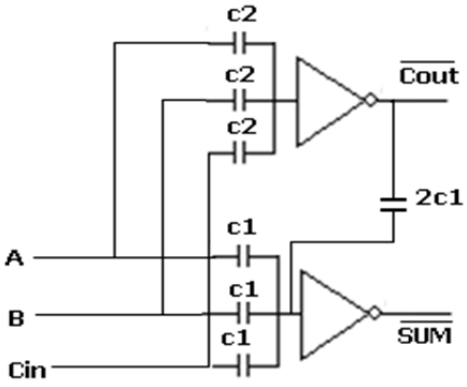


Fig. 1(e) The 4 Transistors full adder (4T)

Fig. 1 Full adder cell of different logic style (a)C-CMOS. (b) CPL. (c) The Hybrid full adder (d) 10T, (c) previous 4T

## III. Proposed Full Adder Cells

The Majority based full adder is based on low power design of Majority Not Function with classical CMOS inverter and capacitors [11]. The main reasons which attribute to low power consumption by Majority based full adder are: 1) low switched capacitance reduction due to its few transistor count, 2) the ability of working at ultra-low

power supply because of having just two transistors from power supply to the ground and taking an advantage from using two robust CMOS inverters in its design, 3) and finally elimination of short circuit current due to its ability in working at low voltage $V_{dd} \leq V_{tn} + |V_{tp}|$ [8]. Although the Majority based full adder enjoys from many fine design parameters used in its structure for low power application, but this remarkable improvement is achieved at the expense of higher area consumption than 4 inverters, and having capacitance effect on its input capacitors derived by common inputs. As illustrated in [11] each of the Majority based full adder inputs are connected to two capacitors which caused to have a charge sharing between these capacitors and a reduction in whole circuit reliability.

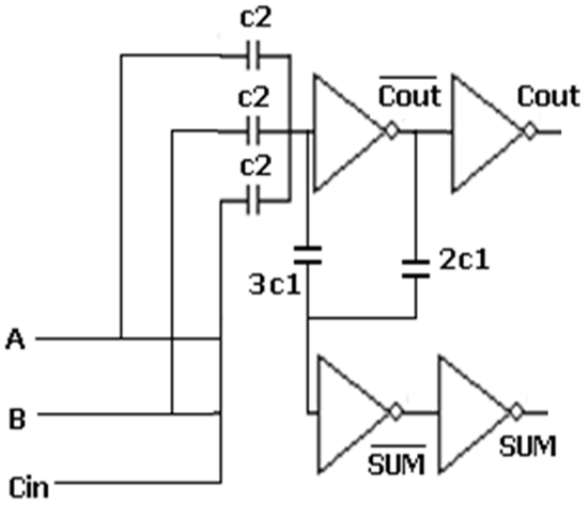


Fig.2: The proposed full adder cell

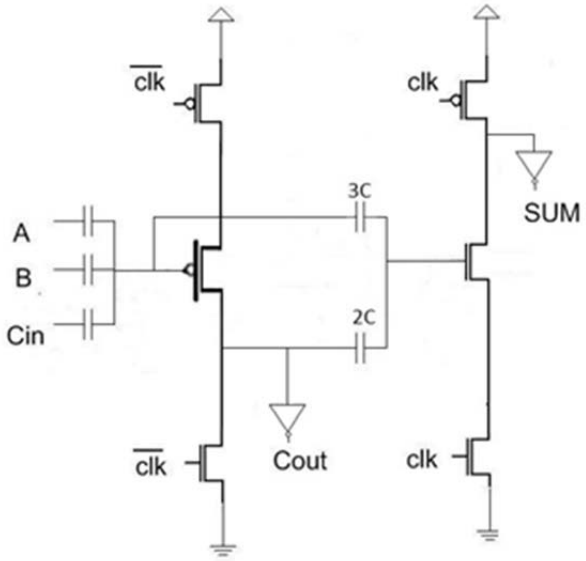


Fig.3: Proposed full-adder cell

As it was cited in [12], instead of using three input capacitors in all over the circuit whenever an universal function is needed, by having a single such capacitors network and using it for all the universal function in the circuit, the mentioned two main disadvantages degrade by a remarkable amount. The majority based full adder uses two Majority Not Function with different number of inputs which does not let us employ such technique for reducing the number of capacitors and eliminating the charge sharing, but an alternative method can be done for this design.

As it was mentioned in [11], each capacitor has one vote in its Majority Not Function, so those two input capacitors which were derived by $\overline{Cout}$ could be substituted by one capacitor with two votes which means that substitute it by a capacitor with 2 times higher in its capacitance value. In order to have a circuit with lower capacitors, those three input capacitors, shown in Fig. 1 could be substituted by a capacitor with 3 times higher in its capacitance value. Fig.2 shows the new structure of the majority based adder, this new 3 times higher capacitor could be derived by the voltage dropped on the gates of first inverter. Because each input capacitor of the first inverter has one vote for the first Majority Not Function, then the voltage dropped on the gates of inverter is the sum of the votes of the inputs, so for the second inverter one capacitor with three times higher in its value could be implied for transferring the sum of the votes of the inputs to the second Majority Not Function. Fig. 3 illustrates the COMS dynamic implementation of the proposed full adder.

It is obvious that with this new design, area consumption is reduced due to the use of one capacitor instead of three capacitors, and finally for eliminating the second disadvantage of the previous Majority based full adder, none of the input signals drive more than one capacitor which results in improving the reliability of the whole circuit. Each input is dedicated to one input capacitor and there is not any fan-out problem for the drivers of the adder and the charge sharing between the input capacitors does not occur which causes to have a new Majority based full adder with higher reliability. In addition to those reductions in the drawbacks of previous Majority based full adder, the new circuit also enjoys from all of the perfect design parameters in its structure for the low power application, such as transistor count.

## IV. Simulation Result

Exhaustive simulation using HSpice have been performed on four circuits and the proposed Majority based full-adder. The technology being used is 0.18µm. The threshold voltages of the NMOS and PMOS transistors are around 0.39 and 0.42 *V*. The supply voltage is 0.8V. By optimizing the transistor sizes of full adders considered, it is possible to reduce the delay of all adders without significantly increasing the power consumption, and transistor sizes can be set to achieve minimum PDP. The outputs of new Majority based full adder are $\overline{\text{Cout}}$ and $\overline{\text{SUM}}$ , so two Inverters are attached to the adder to make it comparable with the previous conventional full adder cells and delay, power and PDP comparisons are performed with these two extra inverters.

Capacitors are implemented in two ways. MIMCAP (Metal-Insulator-Metal Capacitance) technology consumes an enormous chip area but, majority based full adder's capacitors have been implemented using the MOS

capacitors (MOSCAP) available in the 0.18µm CMOS process technology [11].

The results for delay, power consumption, and PDP are shown in Table. 1. For instance, by using 0.8v power supply, the new Majority based full adder consumes 16%, 35%, 14%, 5% less power than C-CMOS, CPL Hybrid, MBFA (Majority based full adder). The delay of new Majority based full adder cell exhibits acceptable value in comparison with the other cells. The CPL is the fastest adder among so many state-of-the-art adder cells.

Table.1 Simulation results for the proposed full adder in 0.18 µm Technology and 0.8V, Vdd.

| DESIGN | Power(µw) | Delay(ns) | PDP(fJ) |
|---|---|---|---|
| C-CMOS | 0.6126 | 0.681 | 0.4172 |
| CPL | 0.8005 | 0.51 | 0.4083 |
| Hybrid | 0.5978 | 0.672 | 0.4017 |
| MBFA | 0.5451 | 0.687 | 0.3745 |
| Proposed | 0.5137 | 0.679 | 0.3488 |

## IV. CONCLUSIONS

A new dynamic full adder cell based on Majority Function is proposed. This new design enjoys low power and high performance operation. A widely comparison to the state of the art designs cited in the VLSI literature illustrates a significant improvement in terms of power dissipation and Power-Delay product (PDP) parameter. The number of transistors used is significantly reduced resulting in a great reduction in switching activity. Besides, due to its dynamic characteristic, short circuit current is eliminated. This considerable reduction in power dissipation as well as some techniques to enhance the speed of the design leads to the best PDP.

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